REMARKS

Claims 1-4 have been amended and new claim 31 has been added to complete the scope of applicants' protection.

Examination on the merits is requested.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) A semiconductor device including a CMOS circuit having an NTFT and a PTFT, each of the NTFT and the PTFT including an active layer, an insulation film in contact with the active layer, and a wiring in contact with the insulation film, wherein

only the NTFT includes a side wall on a side of the wiring,

the active layer of the NTFT includes a channel forming region and at least three kinds of impurity regions each containing an element belonging to the group 15 at a different concentration,

the impurity region in contact with the channel forming region among the three kinds of impurity regions overlaps by way of the insulation film with the side wall,

the active layer of the PTFT includes a channel forming region and two kinds of impurity regions each containing an element belonging to the group 13 at an identical concentration, and

an element used for crystallization of the active layer of the NTFT and the active layer of the PTFT is present at a concentration [of 1×10^{17} to] not greater than 1×10^{20} atoms/cm^3 in one of the impurity region most remote from the channel forming region of the NTFT and in one of the impurity region most remote from the channel forming region of the PTFT.

2. (Amended) A semiconductor device having a CMOS circuit having an NTFT and a PTFT, each of the NTFT and the PTFT including an active layer, an insulation film in contact with the active layer and a wiring in contact with the insulation film, wherein

only the NTFT includes a side wall on a side of the wiring,

the active layer of the NTFT includes a structure in which a channel forming region, a first impurity region, a second impurity region and a third impurity region are arranged in this order,

each of the first impurity region, the second impurity region and the third impurity region contains an element belonging to the group 15 at a different concentration,

the first impurity region overlaps by way of the insulation film with the side wall,

the active layer of the PTFT includes a structure in which a channel forming region, a fourth impurity region and a fifth impurity region are arranged in this order,

each of the fourth impurity region and the fifth impurity region contains an element belonging to the group 13 at an identical concentration and

an element used for the crystallization of the active layer is present at a concentration [of 1 x 10^{17} to] not greater than 1 x 10^{20} atoms/cm^3 in the third impurity region and the fifth impurity region.

3. (Amended) A semiconductor device having a CMOS circuit having an NTFT and a PTFT each of the NTFT and the PTFT including an active layer, an insulation film in contact with the active layer and a wiring in contact with the insulation film, wherein

only the NTFT includes a side wall on a side of the wiring,

the active layer of the NTFT includes a channel forming region and at least three kinds of impurity regions each containing an element belonging to the group 15 at a different concentration,

the concentration of the element belonging to the group 15 is higher as the distance from the channel forming region is greater in at least three kinds of impurity regions,

the active layer of PTFT includes a channel forming region and two kinds of impurity regions containing an element belonging to the group 13 at an identical concentration, and

the active layer of PTFT includes a channel forming region and two kinds of impurity regions containing an element belonging to the group 13 at an identical concentration, and in which

an element used for the crystallization of the active layer is present at a concentration [of 1×10^{17} to] not greater than 1×10^{20} atoms/cm^3 in the impurity region most remote from the channel forming region of the NTFT and in the impurity region most remote from the channel forming region of the PTFT.

4. (Amended) A semiconductor device including a CMOS circuit having an NTFT and a PTFT each of the NTFT and the PTFT including an active layer, an insulation film in contact with the active layer and a wiring in contact with the insulation film, wherein

only the NTFT includes a side wall on a side of the wiring,

the active layer of the NTFT has a structure in which a channel forming region, a first impurity region, a second impurity region and a third impurity region are arranged in this order,

each of the first impurity region, the second impurity region and the third impurity region contains identical impurities at a different concentration,

the concentration of the impurities is higher in the order of the first impurity region, the second impurity region and the third impurity region,

the active layer of the PTFT has a structure in which a channel forming region, a fourth impurity region and a fifth impurity region are arranged in this order,

each of the fourth impurity region and the fifth impurity region contains an element belonging to the group 13 at an identical concentration, and

an element used for the crystallization of the active layer of the NTFT and the active layer of the PTFT is present at a concentration [of 1×10^{17} to] not greater than 1×10^{20} atoms/cm^3 in the third impurity region and the fifth impurity region.